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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/615,920

07/10/2003

Keiji Hosotani

240063US2

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22850

7590

03/02/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.  
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ALEXANDRIA, VA 22314

EXAMINER

HUYNH, ANDY

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/615,920	HOSOTANI ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	BW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8 is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☒ Claim(s) 3-7 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>10/07/2003</u> . | 6) <input type="checkbox"/> Other: ____  |

## **DETAILED ACTION**

Claims **1-8** are pending in this application is acknowledged.

### ***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in JAPAN, 2002-201166 on 07/10/2002.

### ***Information Disclosure Statement***

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on October 07, 2003. The references cited on the PTOL 1449 form have been considered.

### ***Claim Objections***

Claim **1** is objected to because of the following reasons.

In lines 23-24, "the pattern" of said tunnel magnet-resistive element should read --"a pattern" of said tunnel magnet-resistive element--.

***Claim Rejections - 35 U.S.C. § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims **1 and 2** are rejected under 35 U.S.C. 102(a) as being anticipated by Ikeda et al. (US Pub: 2002/0041515 A1 hereinafter referred to as "Ikeda").

Regarding claim 1, Ikeda discloses in Figs. 16 and 19 and related texts as set forth in paragraph [0125] and [0146]-[0150] a magnetic memory device comprising:

a semiconductor substrate (1);

a transistor, having a gate electrode (4), formed above said semiconductor substrate;

a tunnel magneto-resistive element/a TMR film (30) formed above an interlayer dielectric film covering said transistor of said semiconductor substrate;

a first wiring line/a source electrode (12) and a drain electrode (13) buried in said interlayer dielectric film and connected to a source (2)/drain (3) diffusion layer of said transistor;

a second wiring line/a write line (10) buried under said tunnel magneto-resistive element while overlying said first wiring line/the source electrode (12) and a drain electrode (13) in said interlayer dielectric film, to provide a current magnetic field to said tunnel magneto-resistive element during writing; and

a third wiring line/a bit line (6) connected to an upper surface of said tunnel magneto-resistive element/the TMR film and provided to cross said second wiring line/the write line, to

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provide a current magnetic field to said tunnel magneto-resistive element/the TMR film during writing and also to cause a cell current to flow during reading,

wherein said second wiring line/the write line (10) is formed and patterned so that its both edges are placed outside the pattern of said tunnel magneto-resistive element/the TMR film (30) (see Fig. 19).

Regarding claim 2, Ikeda discloses in Fig. 19 the device according to claim 1, wherein said first wiring line/the source electrode (12) and the drain electrode (13) is formed by patterned so that its both edges are placed outside of the pattern of said tunnel magneto-resistive element/the TMR film.

#### *Allowable Subject Matter*

Claims 3-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations.

Regarding claims 3, 6 and 7, Ikeda fails to teach the claimed limitation the device according to claim 2, wherein a gate wiring line of said transistor is patterned to pass through a region immediately beneath said tunnel magneto-resistive element while having a width greater than that of said tunnel magneto-resistive element as recited in claim 3.

Regarding claim 4, Ikeda fails to teach the claimed limitation the device according to claim 2, wherein a gate wiring line of said transistor is patterned to extend outside of a region immediately beneath said tunnel magneto-resistive element.

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Regarding claim 5, Ikeda fails to teach the claimed limitation the device according to claim 2, wherein the first and second wiring lines are formed by patterning to pass through a region immediately beneath said tunnel magneto-resistive element while having a width greater than that of said tunnel magneto-resistive element.

Claim 8 is allowed.

The following is a statement of reason for the indication of allowable subject matter:

Claim 8 is allowable over the cited prior art of Ikeda fails to teach or suggest the limitation recited a magnetic memory device comprises all of element regions including a gate wiring line of said transistor, and the source/drain diffusion layer are formed by patterning so that edges thereof are placed outside of a region immediately underlying said tunnel magneto-resistive element, and includes all other limitations in claim 8.

### ***Conclusion***

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

AH

February 12, 2004



Andy Huynh

Patent Examiner